a p-type well formed in the substrate for the NMOS transistor and an n-type well formed in the substrate for the PMOS transistor, the p-type and n-type wells being isolated from one another; and

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respective contact portions for applying to the semiconductor substrate via the wells different bias voltages in a transistor operating state and a transistor standby so that active regions of the different conductivity type transistors are fully depleted simultaneously.

REMARKS

This is in response to the Office Action dated February 25, 2002. Claims 2, 3 and 12-21 have been canceled (claims 12-21 without prejudice in view of the Restriction Requirement), and new claims 22-24 added. Thus, claims 1, 4-11 and 22-24 are pending. Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page(s) is captioned "**Version With Markings To Show Changes Made**."

A proposed drawing correction to Fig. 9 is attached hereto, with the proposed change being shown in red ink.

Claims 6 and 10 stand objected to; see paragraph 3 of the Office Action. It is respectfully submitted that the claims changes herein address and overcome any potential issue in this regard.

Claims 7-10 stand rejected under 35 U.S.C. Section 103(a) as being allegedly unpatentable over Burr in view of Numata. This Section 103(a) rejection is respectfully traversed for at least the following reasons.

Claim 7 requires "an element isolating region formed in the semiconductor layer, and a contact region formed in the element isolating region for connection with a contact portion for applying a bias voltage to a well of the semiconductor substrate, *the well being of the first conductivity type as is the other region of the semiconductor substrate directly under the well*." In other words, the well of the substrate to which the bias is applied is of the *same* conductivity type (e.g., P-type) as the semiconductor substrate. For example, see Fig. 3 of the instant application which illustrates element isolating region 37 formed in semiconductor layer 33, and a contact region 39a formed in the element isolating region. The bias voltage is applied via the contact region to well 31a of the semiconductor substrate 31, the *well 31a being of the first conductivity type as is the other region of the semiconductor substrate 31 directly under the well.* According to the invention of claim 7, the bias voltage is applied to wells adapted to the conductivity type of the transistor (e.g., p well in the case of N-channel transistors, and n well in the case of P-channel transistors). This is an important aspect of the invention of claim 7 that is not disclosed or suggested by the cited art.

Burr discloses an SOI device including a back gate well(s). However, the well in Burr does not provide a well contact using an isolation region as required by claim 7. Moreover, the well in Burr is required to be of a size that roughly covers the lower part of

the channel region and possibly a small portion of the source/drain region – but *not* the whole source/drain region.

Numata in Fig. 20 does disclose a contact 19 that uses an isolation region 12. In Numata, such a contact can be realized since the back gate 11 extends well beyond the source/drain regions 7 (which is not the case in Burr). Moreover, Numata teaches directly away from the invention of claim 7 by requiring that the back gate 11 (n-type) and the substrate 2 (p-type) be of *different* conductivity types (e.g., col. 16, lines 38-41).

The Section 103(a) combination is fundamentally flawed for at least the following reasons. First, the contact 19 of Numata could not be used in Burr due to the small size of Burr's well. Since Burr requires that the well not cover the entire source/drain region(s), it cannot extend beyond the same and thus cannot be in a position to be contacted by a structure such as Numata's contact 19. In other words, if Numata's contact 19 were inserted into Burr's device, it would not contact Burr's well and would be ineffective. One of ordinary skill in the art would not have done this. Second, Numata's back gate 11 and substrate 2 are required to be of different conductivity types. This teaches directly away from the instant invention, which requires that the well and underlying substrate be of the same conductivity type. Thus, even if Numata's contact 19 and back gate 11 were imported into Burr's device, the invention of claim 7 still would not be met. Third, it can be seen from the above that the transistors of Burr and Numata are much different in detailed structure (e.g., different components have different conductivity types, different sizes and goals, etc.). There is no suggestion or motivation present in the art of record which would have caused one of ordinary skill in the art to

have mixed and matched the various features of Burr and Numata as alleged in the Office Action. Accordingly, it is respectfully submitted that claim 7 as amended defines over the cited art.

Claim 1 stands rejected under 35 U.S.C. Section 103(a) as allegedly unpatentable over Burr in view of Numata as applied to claim 7, and further in view of Yamaguchi. This Section 103(a) rejection is respectfully traversed for at least the following reasons.

The combination of Burr and Numata is fatally flawed for the reasons discussed above. For at least these reasons, claim 1 also defines over the art of record. Additionally, claim 1 requires applying to the semiconductor substrate different bias voltages in an operating state and a standby state. In certain instances, this can decrease OFF current thereby reducing power consumption and/or controlling the floating effect. Burr and Numata fail to disclose or suggest this (the Office Action appears to acknowledge this). While Yamaguchi does disclose changing the potential of a substrate bias in standby and active states, there is no well formed in the substrate under an oxide film of an SOI structure. Yamaguchi is unrelated to Burr and Numata in this regard, and the alleged combination is thus improper. Hindsight is not permissible.

New claims 22-24 state that the bias voltage for a pair of the transistors of different conductivity types is/are changed between the active and standby states so that active regions of the different conductivity type transistors are fully depleted simultaneously. The cited art fails to disclose or suggest this. Fig. 15 of Yamaguchi illustrates that the threshold voltage and the current supplying drivability can be changed by fully depleting one of the transistors (NMOS), but the other (PMOS) cannot be fully

depleted since the bias voltage in the active and standby states is/are applied to the substrate having both N-channel and P-channel transistors thereon. In other words, Yamaguchi fails to disclose or suggest active regions of transistors of two conductivity types fully depleted simultaneously. Thus, even if the art was combined as alleged in the Office Action (which applicant believes would be incorrect in any event), the invention of these claims still would not be met).

For at least the foregoing reasons, it is respectfully requested that all rejections be withdrawn. The application is believed to be in condition for allowance. If any minor matter remains to be resolved, the Examiner is invited to telephone the undersigned with regard to the same.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

Please cancel claims 2, 3 and 12-21.

1. (Amended) A semiconductor device comprising:

a MOS transistor formed on a semiconductor layer of an SOI substrate in which the semiconductor layer is formed on a semiconductor substrate of a first conductivity type with the intervention of a buried insulating film, [and]

a contact portion for applying to the semiconductor substrate different bias voltages in an operating state and a standby state of a semiconductor circuit including the MOS transistor[.],

the transistor including source and drain regions of a second conductivity type, a channel of the first conductivity type, and wherein an impurity diffusion layer of the first conductivity type is formed in the semiconductor substrate under at least the entire source, drain and channel regions, so that the impurity diffusion layer is of the same conductivity type as the semiconductor substrate, and

wherein the contact portion for applying the different bias voltages is formed in a device isolation region and comprises a contact hole in the semiconductor layer and the buried insulating film, said contact hole reaching the impurity diffusion layer so that the different bias voltages are applied to the substrate via the impurity diffusion layer.

4. (Amended) A semiconductor device according to claim 1, wherein the impurity diffusion region is formed as a well [is formed] in a surface of the semiconductor substrate which lies under the MOS transistor[formed on the semiconductor layer], the well having an impurity concentration higher than that of the other region of the substrate, and the bias voltages are applied to the well.

6. (Amended) A semiconductor device according to claim 5, wherein a plurality of wells are formed in the semiconductor substrate and the P-type well and the N-type well are substantially electrically isolated from each other.

7. (Amended) A semiconductor device comprising:

a MOS transistor formed on a semiconductor layer of an SOI substrate in which the semiconductor layer is formed on a semiconductor substrate with the intervention of a buried insulating film,

an element isolating region formed in the semiconductor layer, and

a contact region formed in the element isolating region for connection with a contact portion for applying a bias voltage to a well of the semiconductor substrate, the well being of the first conductivity type as is the other region of the semiconductor substrate directly under the well.

8. (Amended) A semiconductor device according to claim 7, wherein [a] the well is formed in a surface of the semiconductor substrate which lies under the MOS transistor

formed on the semiconductor layer, the well having an impurity concentration higher than that of the other region of the substrate, and the bias voltages are applied to the well.

10. (Amended) A semiconductor device according to claim 9, wherein a plurality of wells are formed in the semiconductor substrate and the P-type well and the N-type well are substantially electrically isolated from each other.